Specification

TFT-LCD module

Module(型号)：	024-B2441
Customer（客户）：	
Customer P/N（客户型号）：	

Approved by（批准）：	
Qualified（合格）：	**Unqualified（不合格）：**

PREPARED	CHECKED	APPROVED

Revision history

Date	Version	Revise record	Page	Design by
2020-12-15	A0	Original version		

TABLE OF CONTENT

1.0 General Specifications

ZSX024-B2441 ***is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It iscomposed of a color TFT-LCD panel, driver IC, FPC and a back light unit. The module display area contains*** 240X320 ***pixels .This product accords with RoHS environmentalcriterion.***

Item	Contents	Unit
LCD Type	TFT TRANSMISSIVE Normally White	/
Viewing direction	12 O'CLOCK	O' Clock
Display Colors	262K	
Module outline (W x HxD)	42.72*60.26*2.34	mm
Active area (WxH)	36.72*48.96	mm
Number of Dots	240(RGB) x320	/
Pixel Pitch	0.153*0.153	mm
Backlight Type	4LED in parallel	/
Interface Type	MCU 8BIT	/
Input voltage	2.8	V

2.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Remark
LC Operating Voltage *1)	V_{op}		4.5	V	Ta= 25℃
Operating Temperature	T_{OP}	-20	70	℃	
Storage Temperature	T_{ST}	-30	80	℃	
Operating Ambient Humidity *2)	Hop	10	*3)	%RH	*3)
Storage Humidity	Hst	10	*3)	%RH	*3)

Note: **[VSS = GND = 0V]**

*1) Liquid Crystal driving voltage: Due to the characteristics of LC Material, this voltage varies with environmental temperature.

*2) Temp≤60℃ 90% RH MAX

*3) Non-condensation

3.0 ELECTRICAL CHARACTERISTICS

Recommend Parameters for Electrical Characteristics

Parameter	Symbol	Value	Unit	Remark
		Reference		
TFT Gate ON Voltage	VGH	12~18	V	Note1
TFT Gate OFF Voltage	VGL	-10~-6	V	Note2
TFT Common Electrode Voltage	VCOM	-2~5	V	Note3
TFT Kick-Back Voltage Max	ΔVp Max	1.0~1.6	V	
TFT Kick-Back Voltage Min	ΔVp Min	0.6~1.2	V	

Note: :

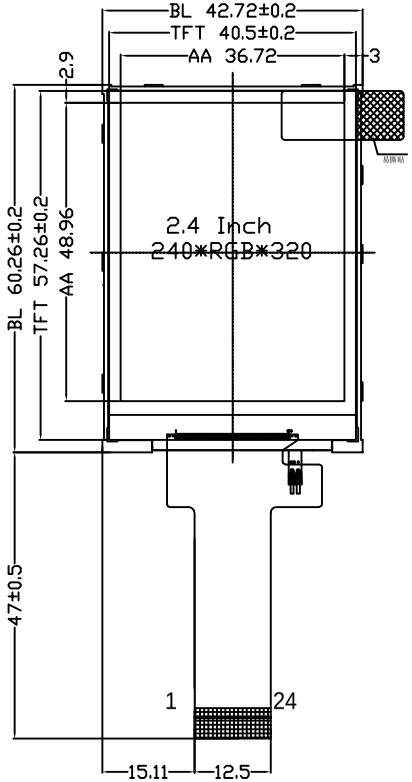
1. V_{GH} is TFT Gate operating voltage.
2. V_{GL} is TFT Gate operating voltage. The low voltage level of V_{GL} signal must be fluctuate with same phase as V_{com}, the storage capacitance structure of the product is storage on common.
3. V_{com} must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc., We just kindly recommend the setting-voltages the reference value.

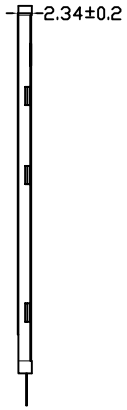
In order to get the optimized display quality, the setting-voltage should be changed according to customer's developing condition. (The display quality could be changed by customer's setting –voltage.)

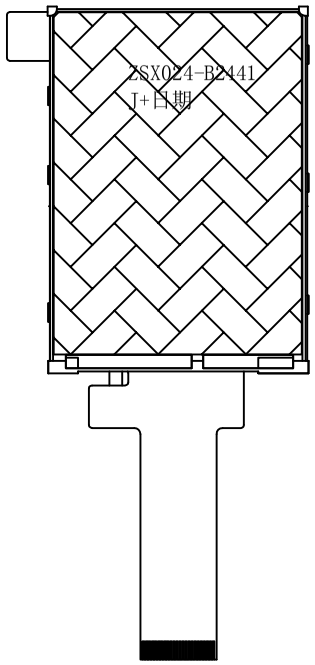
4.0 BACKLIGHT CHARACTERISTICS

Item	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Condition*
Forward voltage	*Vf*	3.0	3.1	3.3	V	If=80mA
Luminance	*Lv*	-	250	-	cd/m2	If=80mA
Number of LED	--	4			Piece	--
Connection mode	*P*	Parallel			--	--

版本	更 改 内 容	拟定	日期
01	First Issue		2020/05/06



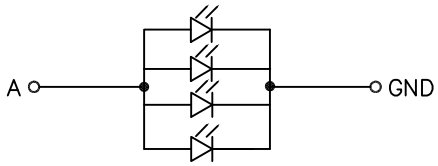




PIN 1	LEDK
PIN 2	LEDA
PIN 3	GND
PIN 4	VCI 3.3V
PIN 5	IOVCC
PIN 6	NC
PIN 7	CS
PIN 8	RESET
PIN 9	RS
PIN 10	WR
PIN 11	RD
PIN 12	DB7
PIN 13	DB6
PIN 14	DB5
PIN 15	DB4
PIN 16	DB3
PIN 17	DB2
PIN 18	DB1
PIN 19	DB0
PIN 20	GND
PIN 21	NC
PIN 22	NC
PIN 23	NC
PIN 24	NC

技术要求:

1) 液晶显示模式: 2.4''TFT Transmissive
2) 显示颜色：262K
3) 视角：12 O'CLOCK
4) 点阵：240(RGB)X320 DOTS
5)驱动芯片型号: ST7789V
6)背光: LED WHITE
7)工作温度:-20°C-----70°C
储存温度:-30°C-----80°C
8)产品符合;ROHS标准



VF:2.9~3.0 IF:80MA

第三视角:

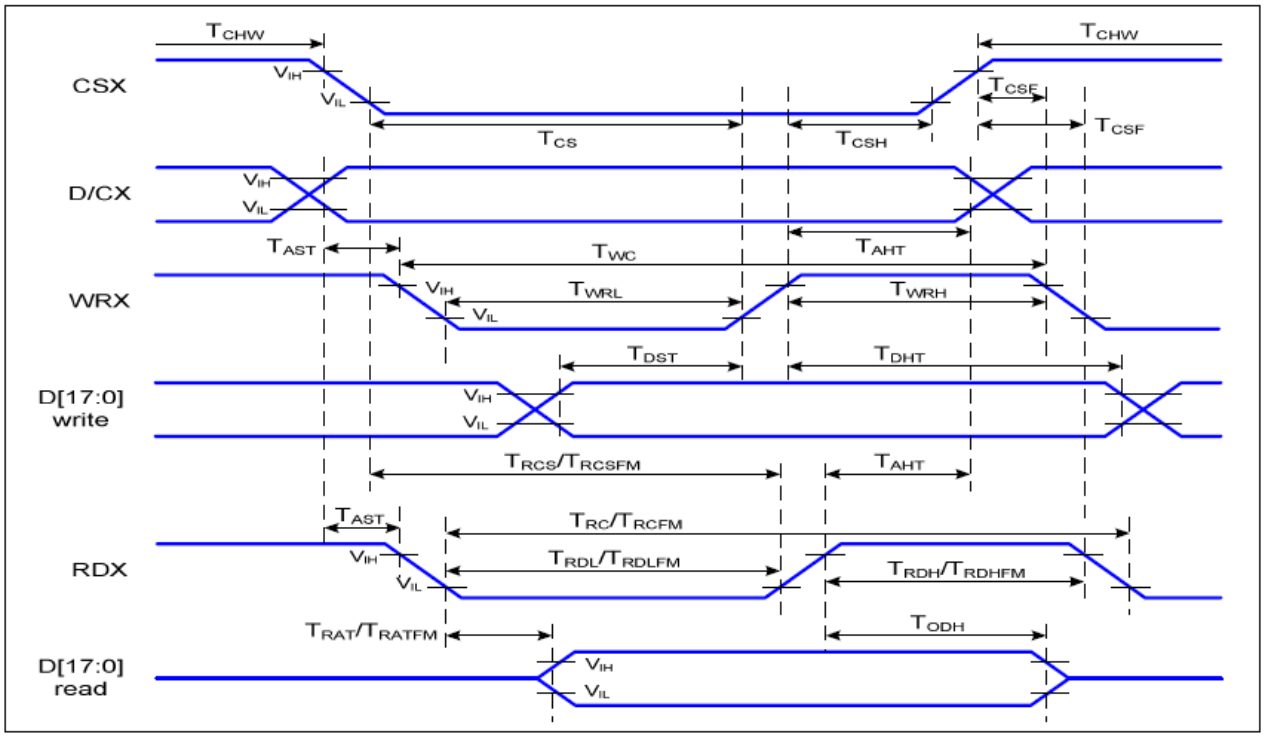
产品型号:	024-B2441				
部品型号:	LCM外形图			核准:	
版本:	0A	单位:	mm	审核:	
日期:		比例:	1:1	设计:	
UNMRKED TOLERANCE:±0.20 mm				页码:	1 OF 1

6.0 INTERFACE PIN CONNECTIONS

1	**LEDK**	**Back light power supply negative**
2	**LEDA**	**Back light power supply positive**
3	**GND**	**Ground**
4	**VCI-3.3V**	**Power supply**
5	**IOVV**	**Power supply**
6	**NC**	**NC**
7	**CS**	**Chip selection pin low:enable high:disable**
8	**RESET**	**Reset pin**
9	**RS**	**Display data/command selection pin in parallel interface**
10	**WR**	**Write enable in MCU parallel interface**
11	**RD**	**Read enable in 8080 MCU parallel interface**
12	**DB7**	**Data**
13	**DB6**	**Data**
14	**DB5**	**Data**
15	**DB4**	**Data**
16	**DB3**	**Data**
17	**DB2**	**Data**
18	**DB1**	**Data**
19	**DB0**	**Data**
20	**GND**	**Ground**
21	**NC**	**NC**
22	**NC**	**NC**
23	**NC**	**NC**
24	**NC**	**NC**

6. 1 Timing characteristics

6.1.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select “H” pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse “H” duration	15		ns	
	T_{WRL}	Control pulse “L” duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF

	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Table 4 8080 Parallel Interface Characteristics

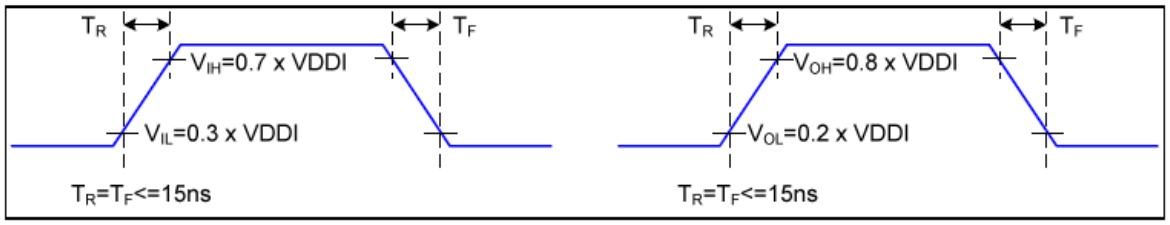


Figure 2 Rising and Falling Timing for I/O Signal

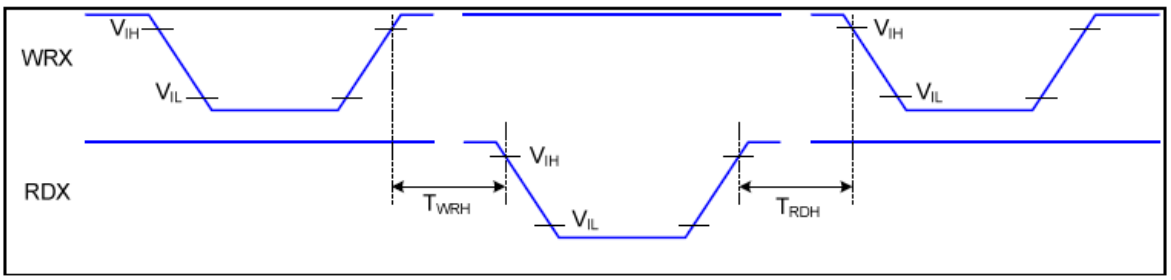


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.1.2 **Reset Timing:**

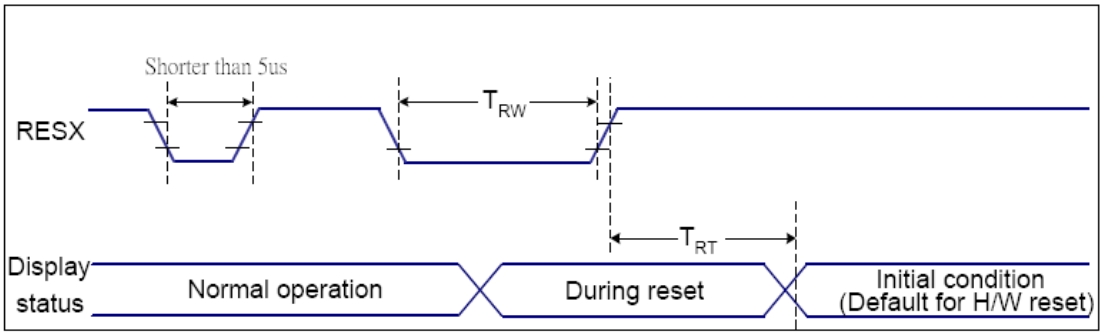


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 8 Reset Timing

6.2. **Write cycle sequence**

The write cycle means that the host writes information (command / data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (DCX, RDX, WRX) and data signals (DB[17:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

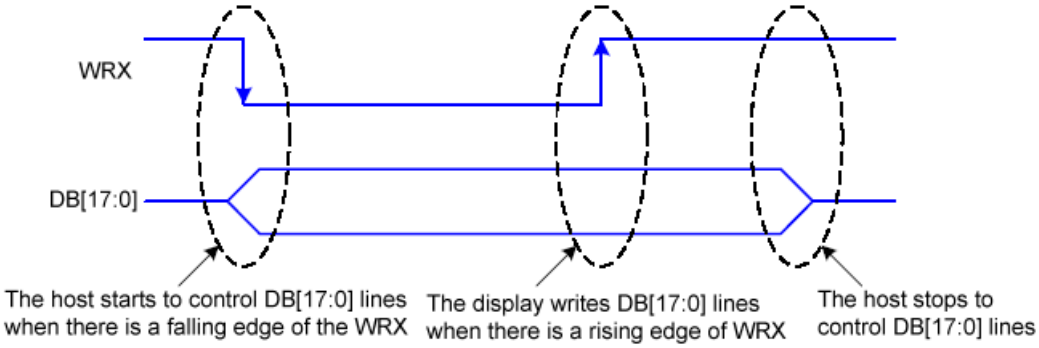


Figure 8 8080-Series WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped).

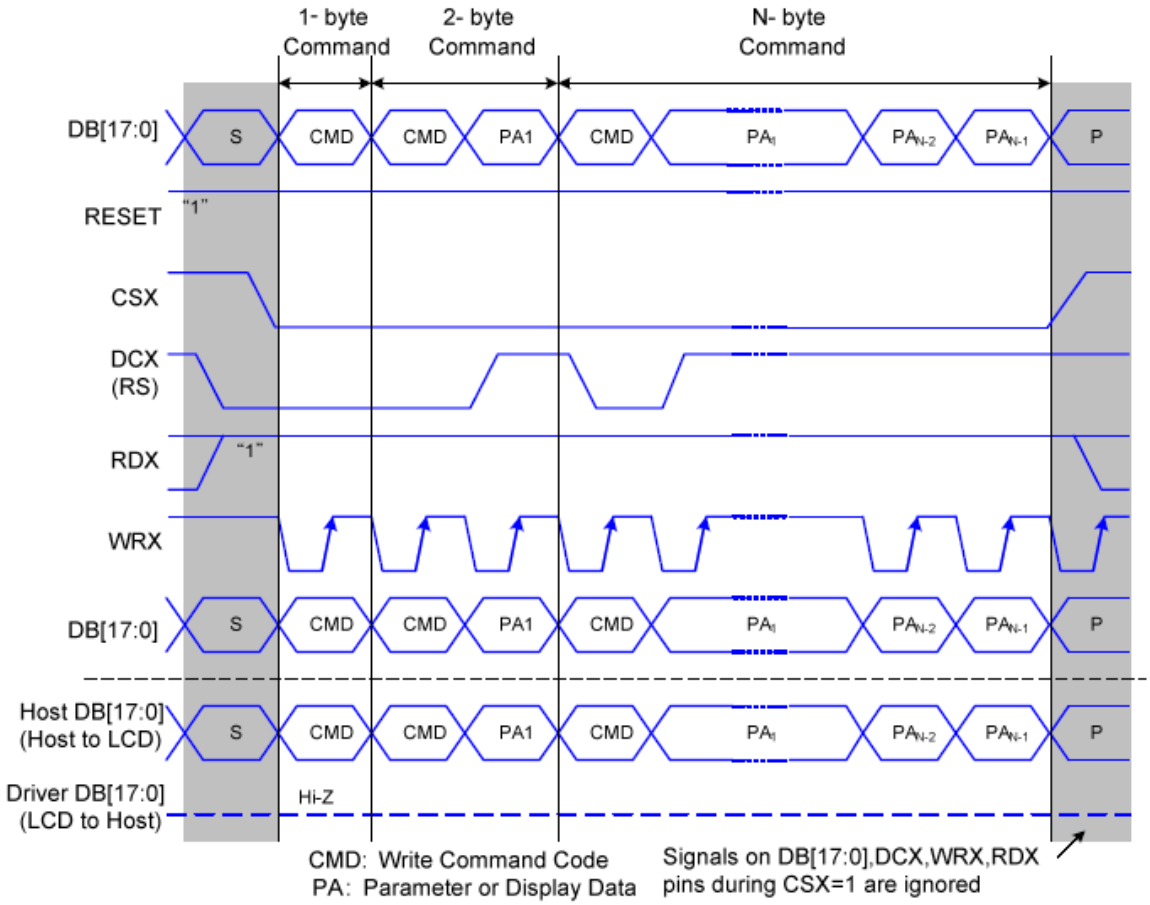


Figure 9 8080-Series Parallel Bus Protocol, Write to Register or Display RAM

6.3. **Read cycle sequence**

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

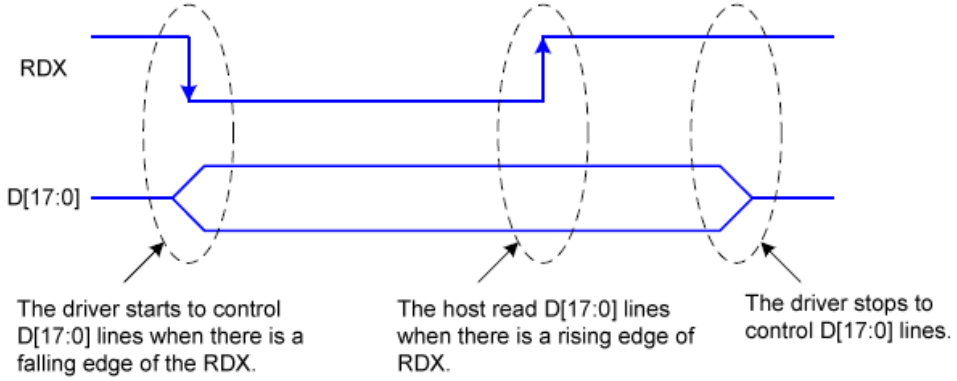


Figure 10 8080-series RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).

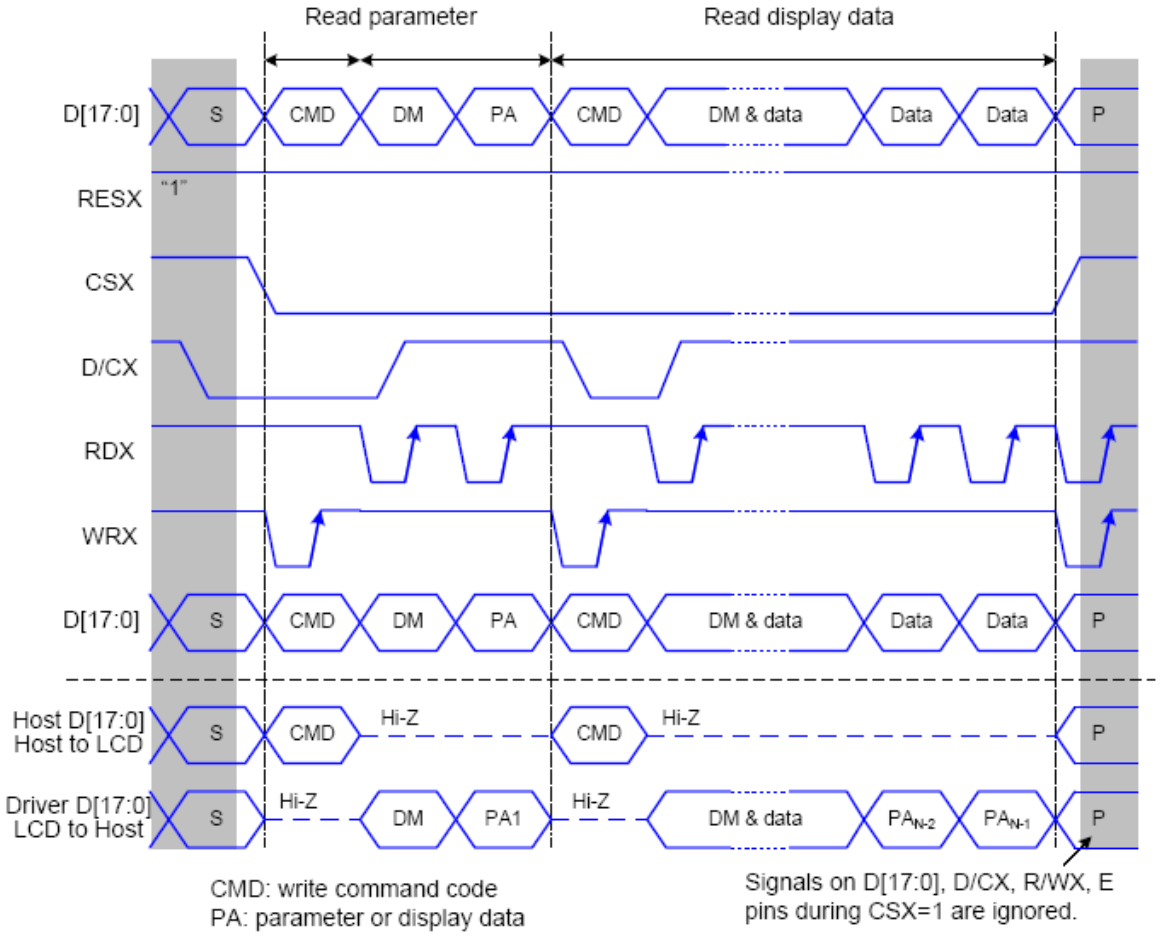


Figure 11 8080-series parallel bus protocol, read data from register or display RAM

7. ELECTRO-OPTICAL CHARACTERISTICS

4.1 Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T(%)	—	—	(4.50)	—	%	Normal POL
Transmittance (without Polarizer)		T(%)	—	—	(12.20)	—	%	
Contrast Ratio		CR	Θ=0 Normal viewing angle	640	800	—	—	(1)(2)
Response Time		$T_R + T_F$		—	30	40	msec	(1)(3)
Color Gamut		S(%)		54	60	—	%	
Color Chromaticity (CIE1931)	White	W_x		+/-0.02	(0.296)	+/-0.02		(1)(4) CF glass
		Wy			(0.325)			
	Red	Rx			(0.647)			
		Ry			(0.329)			
	Green	Gx			(0.279)			
		Gy			(0.550)			
	Blue	Bx			(0.134)			
		By			(0.123)			
Viewing Angle	Hor.	Θ_L	CR>10	—	45	—		Viewing Angle base on using Normal Polarizer， Reference Only
		Θ_R		—	45	—		
	Ver.	Θ_U		—	35	—		
		Θ_D		—	15	—		
Optima View Direction		12						(5)

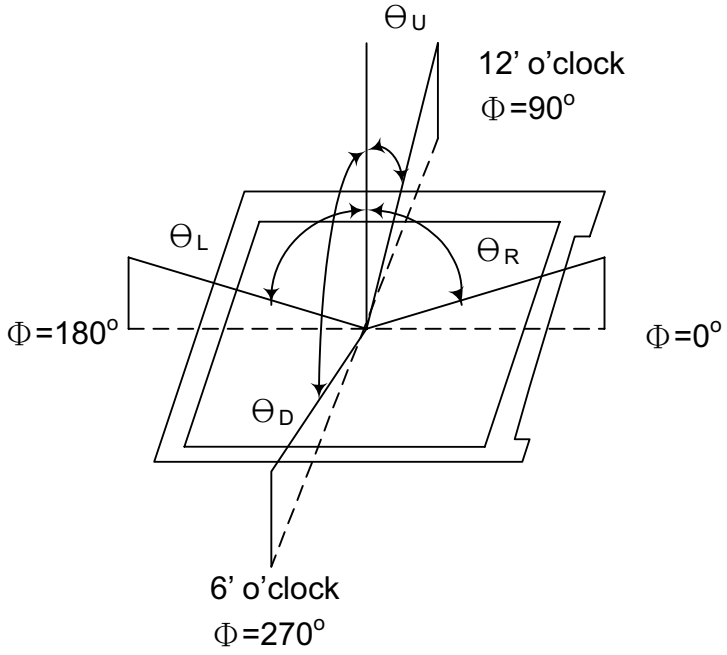
4.2 Measuring Condition

- ■ Measuring surrounding : dark room
- ■ Ambient temperature : 25±2°C
- ■ 15min. warm-up time.

4.3 Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1) Definition of Viewing Angle:

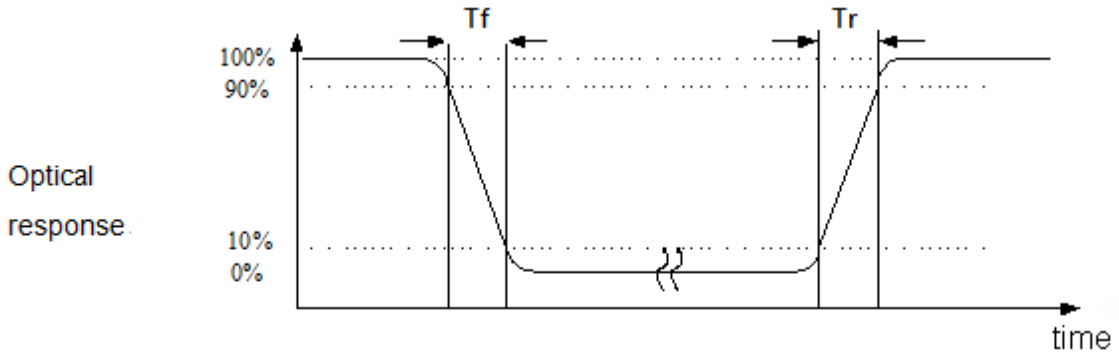


Note (2) Definition of Contrast Ratio (CR):

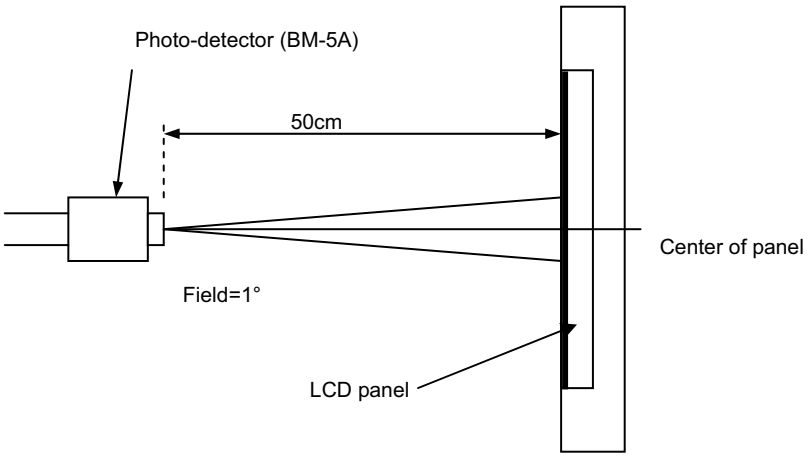
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time: Sum of T_R and T_F



Note (4) Definition of optical measurement setup



8. RELIABILITY

RELIABILITY TEST ITEMS

No.	Item	Conditions	Remark
1	High Temperature Storage	Ta=+80°C, 240hrs	
2	Low Temperature Storage	Ta=-30°C, 240hrs	
3	High Temperature Operation	Ta=+70°C, 240hrs	
4	Low Temperature Operation	Ta=-20°C, 240hrs	
5	High Temperature and High Humidity (Operating)	Ta=+60°C, 90%RH, 240hrs	

Note: (1) All tests above are practiced at module type.

(2) There is no display function NG issue occurred, all the cosmetic specification is judged before the reliability stress.