Sipeed M1 Datasheet

v1.12

Key Features:

- CPU : RISC-V Dual Core 64bit, with FPU，400Mhz-500Mhz, Neural network processor
- Image Recognition: QVGA@60FPS/VGA@30FPS
- Voice Recognition: up to 8 microphones
- Deep learning framework: TensorFlow/Keras/Darknet
- Peripheral: FPIOA、UART、GPIO、SPI、I²C、I²S、WDT、TIMER、RTC etc.

UPDATE	
V1.0	2018/10/25 Published original document
V1.1	2019/3/6 Removed M1w description
V1.11	2020/7/30 Modified IOs description & fixed PIN MAP picture
V1.12	2021/10/11 Fixed PIN MAP picture;Add precautions

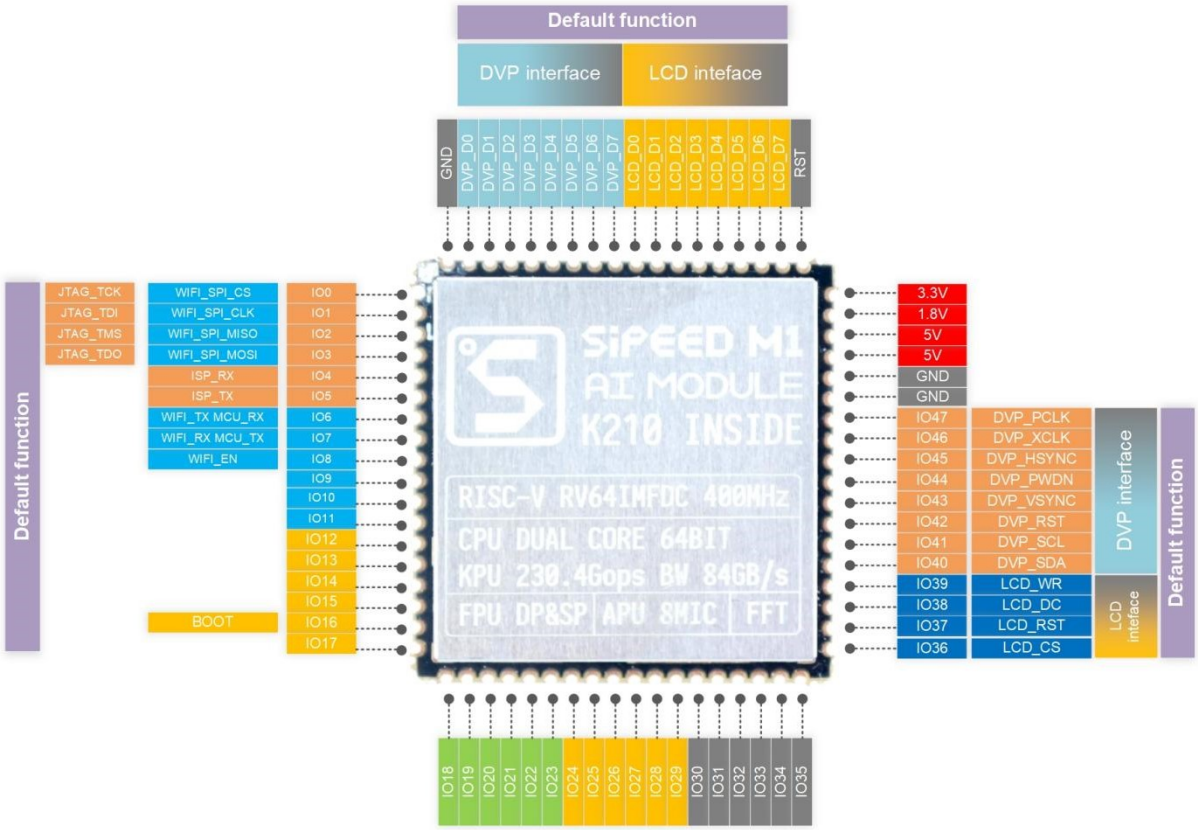
SPECIFICATION	
CPU : RISC-V Dual Core 64bit, 400Mh adjustable	Powerful dual-core 64-bit open architecture-based processor with rich community resources
FPU Specifications	IEEE754-2008 compliant high-performance pipelined FPU
Debugging Support	High-speed UART and JTAG interface for debugging
Neural Network Processor (KPU)	• Supports the fixed-point model that the mainstream training framework trains according to specific restriction rules • There is no direct limit on the number of network layers, and each layer of convolutional neural network parameters can be configured separately, including the number of input and output channels, and the input and output line width and column height • Support for 1x1 and 3x3 convolution kernels • Support for any form of activation function • The maximum supported neural network parameter size for real-time work is 5MiB to 5.9MiB • The maximum supported network parameter size when working in non-real time is (flash size - software size)
Audio Processor (APU)	• Up to 8 channels of audio input data, ie 4 stereo channels • Simultaneous scanning pre-processing and beamforming for sound sources in up to 16 directions • Supports one active voice stream output • 16-bit wide internal audio signal processing • Support for 12-bit, 16-bit, 24-bit, and 32-bit input data widths • Multi-channel direct raw signal output • Up to 192kHz sample rate • Built-in FFT unit supports 512-point FFT of audio data • Uses system DMAC to store output data in system memory
Static Random-Access Memory (SRAM)	The SRAM is split into two parts, 6MiB of on-chip general-purpose SRAM memory and 2MiB of on-chip AI SRAM memory, for a total of 8MiB
Field Programmable IO Array (FPIOA/IOMUX)	FPIOA allows users to map 255 internal functions to 48 free IOs on the chip

Digital Video Port (DVP)	Maximum frame size 640x480
FFT Accelerator	The FFT accelerator is a hardware implementation of the Fast Fourier Transform (FFT)

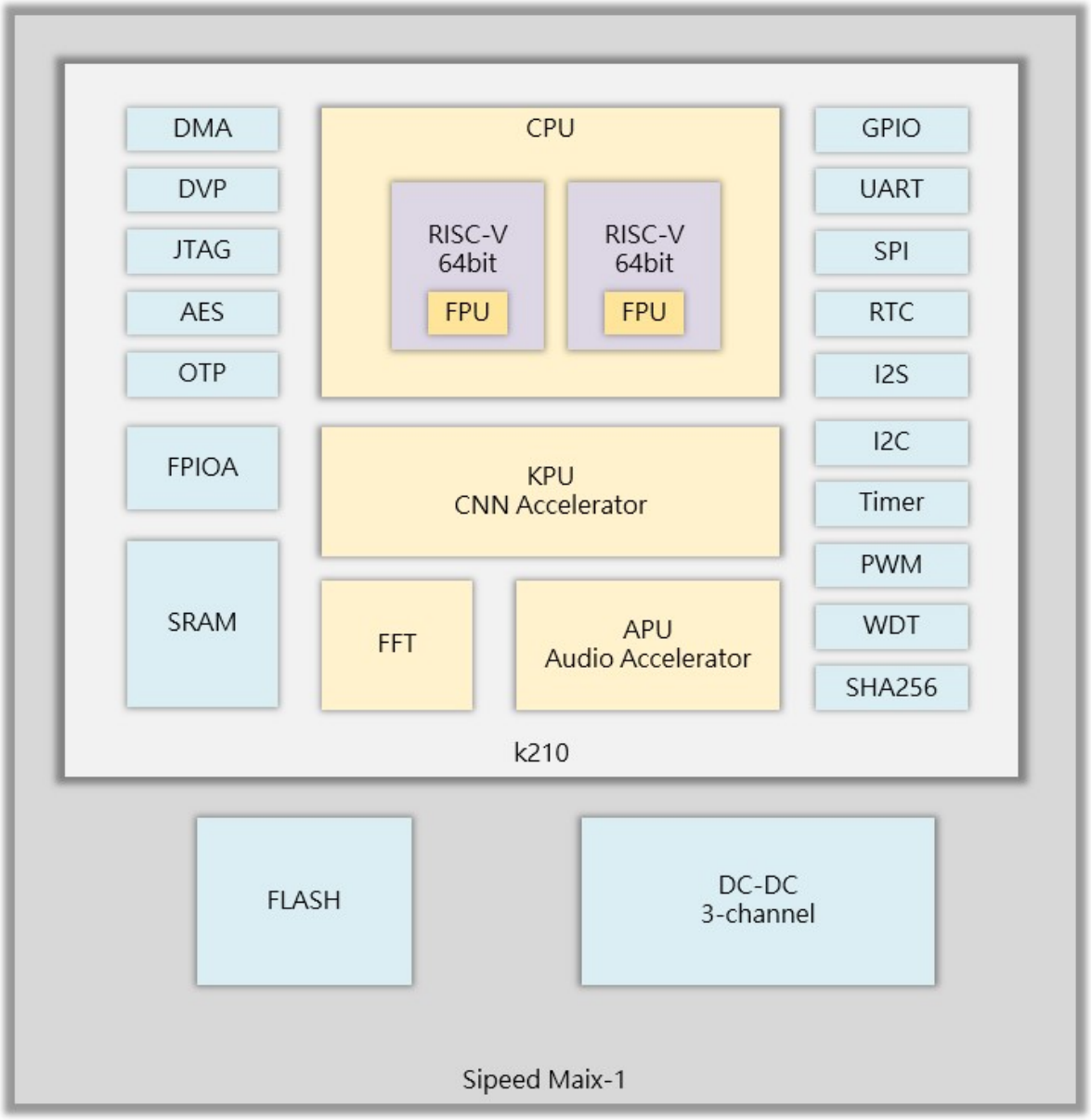
SOFTWARE FEATURES	
FreeRtos & Standard SDK	Support FreeRtos and Standrad development kit.
MicroPython Support	Support MicroPython on M1
Machine vision	Machine vision based on convolutional neural network
Machine hearing	High performance microphone array processor
Maixpy & Maixpy IDE	https://maixpy.sipeed.com/en/

HARDWARE FEATURES	
Supply voltage of external power supply	5.0V ±0.2V
Supply current of external power supply	> 300mA @ 5V
Temperature rise	<30K
Range of working temperature	-30℃ ~ 85℃

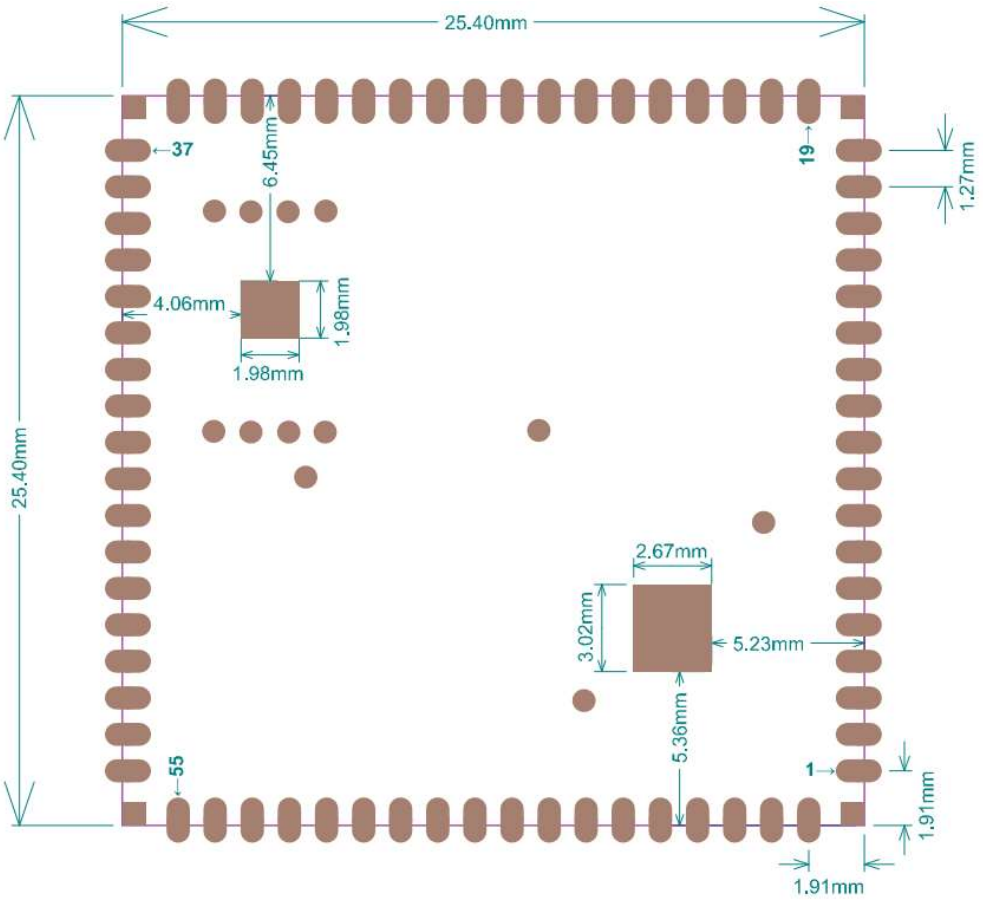
M1 PIN MAP


Default function
DVP interface
LCD inteface
GND
DVP_D0
DVP_D1
DVP_D2
DVP_D3
DVP_D4
DVP_D5
DVP_D6
DVP_D7
LCD_D0
LCD_D1
LCD_D2
LCD_D3
LCD_D4
LCD_D5
LCD_D6
LCD_D7
RST
Default function
JTAG_TCK
JTAG_TDI
JTAG_TMS
JTAG_TDO
WIFI_SPI_CS
WIFI_SPI_CLK
WIFI_SPI_MISO
WIFI_SPI_MOSI
ISP_RX
ISP_TX
WIFI_TX MCU_RX
WIFI_RX MCU_TX
WIFI_EN
BOOT
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO15
IO16
IO17
SiPEED M1
AI MODULE
K210 INSIDE
RISC-V RV64IMFDC 400MHz
CPU DUAL CORE 64BIT
KPU 230.4Gops BW 84GB/s
FPU DP&SP APU 8MIC FFT
3.3V
1.8V
5V
5V
GND
GND
IO47
IO46
IO45
IO44
IO43
IO42
IO41
IO40
IO39
IO38
IO37
IO36
DVP_PCLK
DVP_XCLK
DVP_HSYNC
DVP_PWDN
DVP_VSYNC
DVP_RST
DVP_SCL
DVP_SDA
LCD_WR
LCD_DC
LCD_RST
LCD_CS
DVP interface
LCD inteface
Default function
IO18
IO19
IO20
IO21
IO22
IO23
IO24
IO25
IO26
IO27
IO28
IO29
IO30
IO31
IO32
IO33
IO34
IO35

M1 BLOCK DIAGRAM



SIZE	
Length	25.4mm
Width	25.4mm
Height	3.3 mm



Please download the DXF file from dl.sipeed.com.

Sipeed M1 PIN ASSIGNMENT

#	PIN	#	PIN	#	PIN	#	PIN
1	JTAG_TCK	19	MIC_BCK	37	LCD_CS	55	RST
2	JTAG_TDI	20	MIC_WS	38	LCD_RST	56	LCD_D7
3	JTAG_TMS	21	MIC_DAT3	39	LCD_DC	57	LCD_D6
4	JTAG_TDO	22	MIC_DAT2	40	LCD_WR	58	LCD_D5
5	ISP_RX	23	MIC_DAT1	41	DVP_SDA	59	LCD_D4
6	ISP_TX	24	MIC_DAT0	42	DVP_SCL	60	LCD_D3
7	IO6	25	MIC_LED_DAT	43	DVP_RST	61	LCD_D2
8	IO7	26	SPI0_CS1	44	DVP_VSYNC	62	LCD_D1
9	IO8	27	SPI0_MISO	45	DVP_PWDN	63	LCD_D0
10	IO9	28	SPI0_SCLK	46	DVP_HSYNC	64	DVP_D7
11	IO10	29	SPI0_MOSI	47	DVP_XCLK	65	DVP_D6
12	IO11	30	SPI0_CS0	48	DVP_PCLK	66	DVP_D5
13	LED_G	31	MIC0_WS	49	GND	67	DVP_D4
14	LED_B	32	MIC0_DATA	50	GND	68	DVP_D3
15	LED_R	33	MIC0_BCK	51	5V	69	DVP_D2
16	IO15	34	I2S_WS	52	5V	70	DVP_D1
17	BOOT KEY0	35	I2S_DA	53	1V8	71	DVP_D0
18	IO17	36	I2S_BCK	54	3V3	72	GND

Electrical Characteristics

Parameter	Name	Min	Typ	Max	Unit
3.3V/1.8V IO supply voltage	VDD	-	$3.3/1.8$	-	V
1.8V Digital supply voltage	$DVDD_{1.8V}$	-	1.8	-	V
1.8V Analog supply voltage	$AVDD_{1.8V}$	-	1.8	-	V
0.9V Core supply voltage	$VDD_{0.9V}$	-	0.9	-	V
3.3V IO supply current	$I_{3.3V}$	1	-	-	mA
1.8V Digital supply current	$I_{1.8V}$	1	-	-	mA
1.8V Analog supply current	$I_{1.8V}$	2	-	-	mA
0.9V Core supply current	$I_{0.9V}$	30	-	-	mA
3.3V/1.8V IO input high level	V_{IH}	$0.7 * VDD$	-	-	V
3.3V/1.8V IO input low level	V_{IL}	-	-	$0.3 * VDD$	V
IO High output level	V_{OH}	-	$VDD - 0.3$	-	mV
IO Low output level	V_{OL}	-	0.3	-	mV
IO Input leakage current	I_{IL}	-	**TBD**[*1]	-	nA
IO Input capacitance	C_{PAD}	-	**TBD**	-	pF
Storage Temperature	T_{STR}	-40	25	150	$°C$
Operating Temperature	T_{OPR}	-40	25	125	$°C$

The above information comes from kendryte_datasheet_20181011163248_en.pdf

IO voltage configuration (Hardware)

BANK0 (IO0-IO5) BANK1 (IO6-IO11) BANK2 (IO12-IO17) BANK3 (IO18-IO23) BANK4 (IO24-IO29) BANK5 (IO30-IO35)	3.3V default
BANK6 (IO36-IO41) BANK7 (IO42-IO47)	1.8V default
DVP_D0-DVP_D7 SPI0_D0-SPI0_D7	1.8V only
RST	1.8V only

Programmable Drive Capability

Low level output current

DS[3:0]	Min(mA)	Typ(mA)	Max(mA)
0000	3.2	5.4	8.3
0001	4.7	8.0	12.3
0010	6.3	10.7	16.4
0011	7.8	13.2	20.2
0100	9.4	15.9	24.2
0101	10.9	18.4	28.1
0110	12.4	20.9	31.8
0111	13.9	23.4	35.5

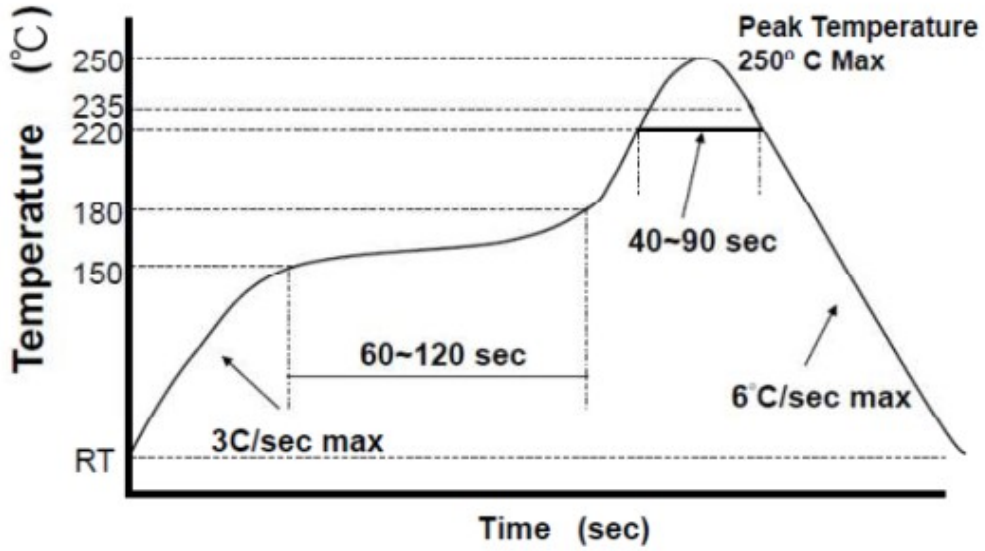
High level output current

DS[3:0]	Min(mA)	Typ(mA)	Max(mA)
0000	5.0	7.6	11.2
0001	7.5	11.4	16.8
0010	10.0	15.2	22.3
0011	12.4	18.9	27.8
0100	14.9	22.6	33.3
0101	17.4	26.3	38.7
0110	19.8	30.0	44.1
0111	22.3	33.7	49.5

The above information comes from kendryte_datasheet_20181011163248_en.pdf

Matters needing attention	
Special pins	IO_16 is used for boot mode selection. During power-on reset, pull high to boot from FLASH and pull low to enter ISP mode. After reset, IO_0, IO_1, IO_2, and IO_3 are JTAG pins. IO_4 and IO_5 are ISP pins.
RST pin	Vrst range : 0 to 1.8V ; Active low ; Do not let the voltage of RST pin be greater than 1.8V
Thermal design	It is recommended to connect the pad on the bottom of the module to a large piece of copper on the bottom plate to help heat dissipation
Electrostatic protection	1. All IO ports and power pins used need to be equipped with ESD diodes 2. All IO ports used need a resistance between 100Ω-1kΩ in series
Precautions for PCB design using this module	https://bbs.sipeed.com/thread/62

REFLOW PROFILE GUIDELINE



RESOURCES	
Official Website	www.sipeed.com
Github	https://github.com/sipeed
BBS	http://bbs.sipeed.com
Wiki	maixpy.sipeed.com
Sipeed Model Store	https://maixhub.com/
SDK Reference	dl.sipeed.com/MAIX/SDK
HDK Reference	dl.sipeed.com/MAIX/HDK
E-mail (Technical Support)	support@sipeed.com
Telegram Link	https://t.me/sipeed
QQ Group	878189804

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