Sipeed M1n Datasheet

v1.0

Key Features:

- CPU : RISC-V 64bit dual-core processor, 400Mhz standard frequency (overclockable)
- Image recognition: QVGA@60FPS/VGA@30FPS
- Voice recognition: supports arrays of up to 8 microphones
- Deep Learning Framework: TensorFlow/Keras/Darknet
- Peripherals: FPIOA, UART, GPIO, SPI, I2C, I2S, WDT, TIMER, RTC etc.

UPDATE	
V1.0	Edited on September 11, 2019 ; Original document

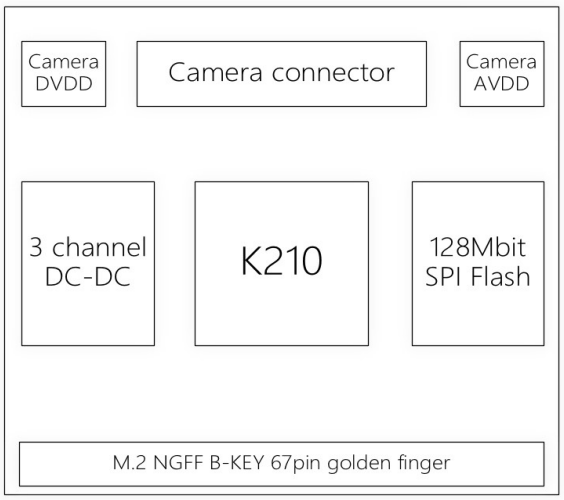
SPECIFICATION	
CPU : RISC-V dual core 64bit, 400Mh adjustable frequency:	Powerful dual-core 64-bit open architecture-based processor with rich community resources
FPU specifications	Meet the IEEE754-2008 standard
Debugging support	High-speed UART and JTAG interface for debugging (only wire bond pads are available)
Onboard camera DVP carrier	24pin 0.5mm pitch FPC carrier; AVDD-3.0V; DVDD-1.3V
Pin out	In addition to the 4 IOs of the JTAG interface, the rest of the IO is exported to the M.2 interface.
Neural Network Processor (KPU)	• Support for the fixed-point model trained by the mainstream training framework in accordance with specific restriction rules • There is no direct limit on the number of network layers, which supports separate configuration of each layer of convolutional neural network parameters, including the number of input and output channels, input and output line width and column height. • Support for two convolution kernels 1x1 and 3x3 • Support for any form of activation function • Maximum support for neural network parameters in real-time operation from 5.5MiB to 5.9MiB • Maximum supported network parameter size when working in non-real time (Flash capacity - software volume)
Audio processor (APU)	• Can support up to 8 audio input streams, ie 4 channels of dual channel • Can support simultaneous sound source pre-processing and beamforming in up to 16 directions • Can support a valid voice stream output • Internal audio signal processing accuracy reaches 16-bit • Input audio signal supports 12-bit, 16-bit, 24-bit, 32-bit precision • Support multi-channel raw signal direct output • Can support audio input up to 192K sample rate • Built-in FFT transform unit to provide 512-point fast Fourier transform for audio data • Store output data into SoC's system memory using system

	DMAC
Static Random Access Memory (SRAM)	The SRAM consists of two parts, 6MiB of on-chip general purpose SRAM memory and 2MiB of on-chip AI SRAM memory, for a total of 8MiB (1Mib is 1 megabyte).
Field Programmable IO Array (FPIOA/IOMUX)	FPIOA allows users to map 255 internal functions to 48 free IOs on the periphery of the chip
Digital Video Interface (DVP)	Maximum support 640X480 and below resolution, configurable per frame size
Fast Fourier transform accelerator	The FFT accelerator implements FFT operations in hardware.

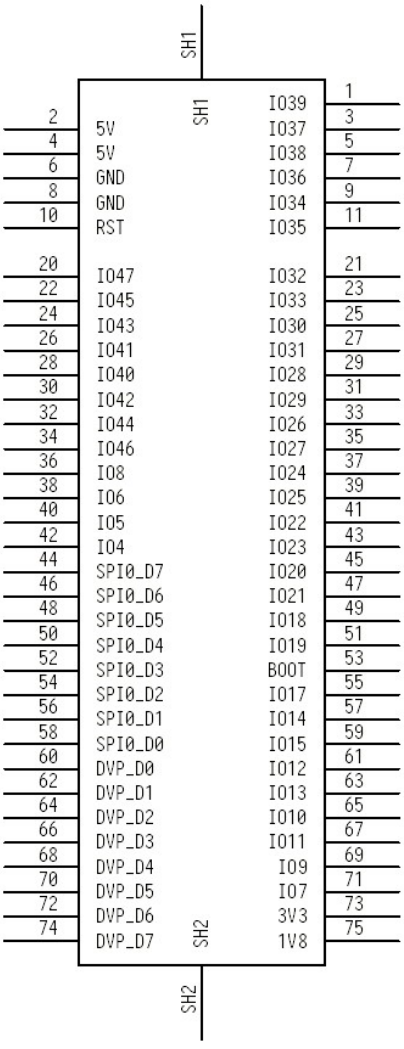
SOFTWARE FEATURES	
FreeRtos & Standard SDK	Support FreeRtos and Standrad development kit.
MicroPython Support	Support MicroPython on M1
Machine vision	Machine vision based on convolutional neural network
Machine hearing	High performance microphone array processor

HARDWARE FEATURES	
External supply voltage requirement	5.0V ±0.2V
External supply current demand	> 300mA @ 5V
Temperature rise	<30K
Range of working temperature	-30℃ ~ 85℃

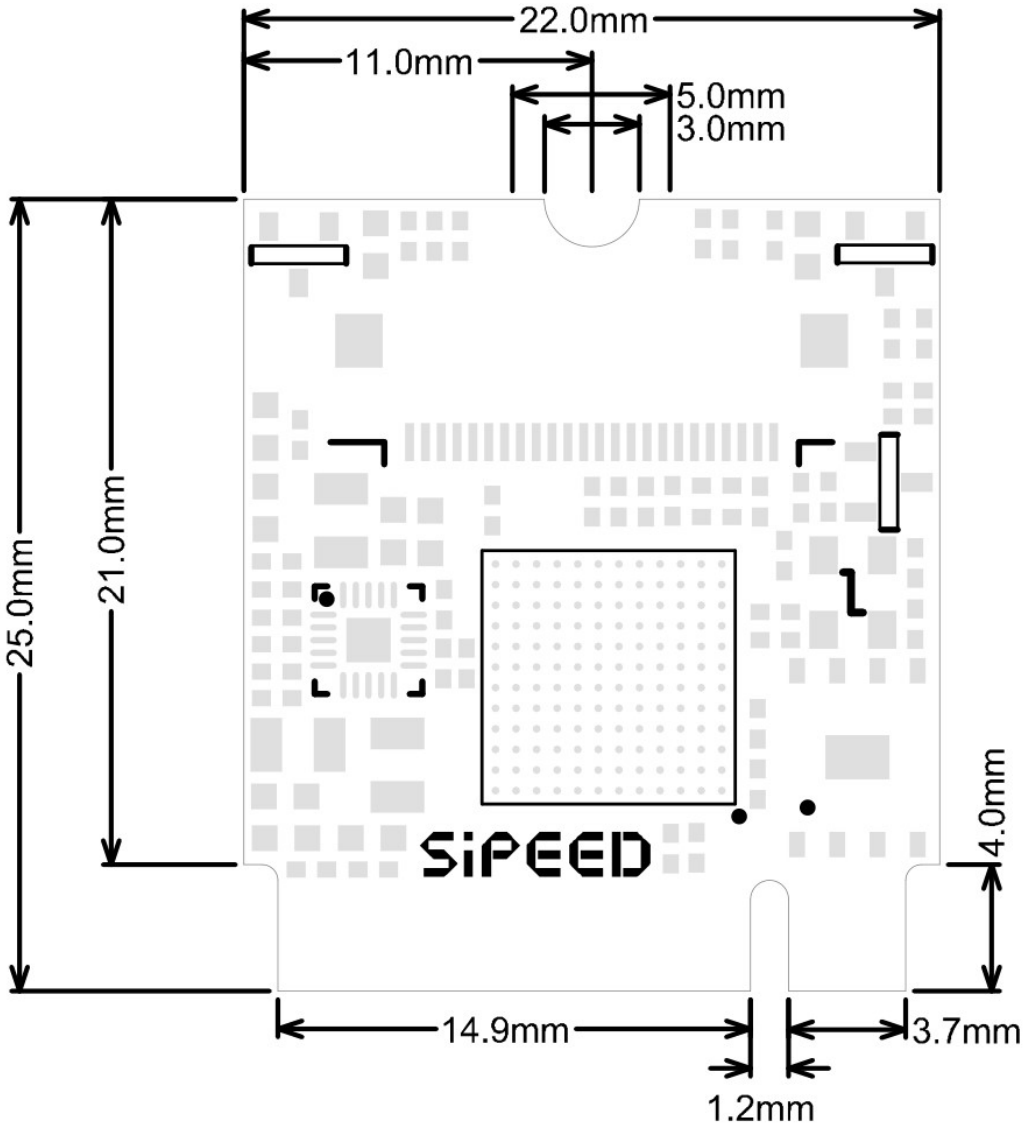
M1n block diagram



M1n pin out



SIZE	
Length	25.0mm
Width	22.0mm
Height	2.7 mm



Matters needing attention	
Boot mode selection	At startup, BOOT(IO16) pin is used to select one of two boot options: ● Boot from main flash memory (Set BOOT pin 3.3V) ● Enter ISP download mode (Set BOOT pin 0V) The pull-up resistance of boot pin needs to be added to the motherboard, and the pull-up voltage is 3.3V
RST pin	Vrst range : 0 to 1.8V ; Active low ; Do not let the voltage of RST pin be greater than 1.8V
Electrostatic protection	1. All IO ports and power pins used need to be equipped with ESD diodes 2. All IO ports used need a resistance between 100Ω-1kΩ in series
Precautions for PCB design using this module	https://bbs.sipeed.com/thread/62

RESOURCES	
Official Website	www.sipeed.com
Github	https://github.com/sipeed
BBS	http://bbs.sipeed.com
Wiki	maixpy.sipeed.com
Sipeed Model Store	https://maixhub.com/
SDK Reference	dl.sipeed.com/MAIX/SDK
HDK Reference	dl.sipeed.com/MAIX/HDK
E-mail(Technical Support)	support@sipeed.com
telgram link	https://t.me/sipeed
QQ Group	878189804

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